



AMENDMENT TO THE CLAIMS

Please amend the presently pending claims as follows:

1. (Currently Amended) A phase-locked loop (PLL) comprising:
  - a range select input;
  - a clock output;
  - a phase/frequency detector having a reference input and a feedback input;
  - a charge pump coupled to an output of the phase/frequency detector;
  - a loop filter coupled to an output of the charge pump; and
  - a voltage-controlled oscillator (VCO) circuit coupled to the loop filter and comprising a plurality of ~~(VCOs)~~ VCOs, which are selectively coupled between the loop filter and the clock output as a function of the range select input and have different output frequency ranges; and
  - a plurality of voltage level shifters, wherein each voltage level shifter is coupled between a respective one of the VCO's and the clock output and is adapted to convert differential signals produced at an output of the respective VCO into a digital logic level signal, and wherein each voltage level shifter comprises a power down input and at least one current source or voltage bias generator, which is enabled and disabled by the power down input.
  
2. (Currently Amended) The PLL of claim 1 wherein each ~~VCO has~~ a VCO voltage level shifter has a voltage level shifter output and the PLL further comprises a multiplexer having a plurality of multiplexer inputs coupled to respective ~~VCO outputs of the plurality of VCOs~~ voltage level shifter outputs, a select input controlled by the range select input and a multiplexer output coupled to the clock output.

3. (Original) The PLL of claim 1 wherein each VCO comprises a power down input coupled to the range select input and at least one current source in the VCO, which is enabled and disabled by the power down input.

4. (Original) The PLL of claim 1 wherein each VCO comprises a power down input coupled to the range select input and at least one bias voltage generator in the VCO, which is enabled and disabled by the power down input.

5. (Cancelled)

6. (Currently Amended) The PLL of claim ~~12~~ 1 wherein the loop filter comprises a resistor connected in series with a programmable capacitor circuit, wherein the programmable capacitor circuit comprises a plurality of capacitors, which are selectively coupled in parallel with one another as a function of the range select input.

7. (Original) The PLL of claim 6 wherein the PLL further comprises a third-order loop filter capacitor circuit coupled in parallel with the series connection of the resistor and the programmable capacitor circuit and having a plurality of third-order capacitors, which are selectively coupled in parallel with one another as a function of the range select input.

8. (Original) The PLL of claim 1 wherein the PLL further comprises a control circuit, which decodes the range select input into a plurality of VCO select signals and a capacitance select signal, wherein each of the VCOs is enabled and disabled as a function of a respective one of the VCO select signals and the loop filter has a capacitance that is selectable as a function of

the capacitance select signal.

9. (Currently Amended) An integrated circuit comprising a phase-locked loop (PLL), which is fabricated on the integrated circuit and comprises a selectable loop filter capacitance and a selectable output frequency range, wherein the PLL further comprises: a clock output; a loop filter providing the loop filter capacitance; a plurality of voltage-controlled oscillators (VCOs), which are selectively coupled between the loop filter and the clock output as a function of a range select input and have different output frequency ranges, and a plurality of voltage level shifters, wherein each voltage level shifter is coupled between a respective one of the VCO's and the clock output and is adapted to convert differential signals produced at an output of the respective VCO into a digital logic level signal, and wherein each voltage level shifter comprises a power down input and at least one current source or voltage bias generator, which is enabled and disabled by the power down input.

10. (Currently Amended) The integrated circuit of claim 9 ~~wherein the PLL further comprises: a range select input, wherein~~ the loop filter capacitance and the output frequency range are selectable as a function of the range select input.

11. (Cancelled)

12. (Currently Amended) The integrated circuit of claim ~~11~~ 9 wherein each ~~VCO has a VCO~~ voltage level shifter has a voltage level shifter output and the PLL further comprises a multiplexer having a plurality of multiplexer inputs coupled to respective voltage level shifter outputs ~~VCO outputs of the plurality of VCOs~~, a select input controlled by the range select input and a multiplexer output coupled to the clock output.

13. (Currently Amended) The integrated circuit of claim ~~11~~ 9 wherein each VCO comprises a power down input coupled to the range select input and at least one current source in the VCO, which is enabled and disabled by the power down input.

14. (Currently Amended) The integrated circuit of claim ~~11~~ 9 wherein each VCO comprises a power down input coupled to the range select input and at least one bias voltage generator in the VCO, which is enabled and disabled by the power down input.

15. (Cancelled)

16. (Currently Amended) The integrated circuit of claim ~~11~~ 9 wherein the loop filter comprises a resistor connected in series with a programmable capacitor circuit, wherein the programmable capacitor circuit comprises a plurality of capacitors, which are selectively coupled in parallel with one another as a function of the range select input.

17. (Original) The integrated circuit of claim 16 wherein the PLL further comprises a third-order loop filter capacitor circuit coupled in parallel with the series connection of the resistor and the programmable capacitor circuit and having a plurality of third-order capacitors, which are selectively coupled in parallel with one another as a function of the range select input.

18. (Currently Amended) The integrated circuit of claim ~~11~~ 9 wherein the PLL further comprises a control circuit, which decodes the range select input into a plurality of VCO select signals and a capacitance select signal, wherein each of the VCOs is enabled and disabled as a function of a respective one of the VCO select signals and the loop filter capacitance is selectable

as a function of the capacitance select signal.

19. (Currently Amended) A method of programming a phase-locked loop, the method comprising:

- (a) receiving a range select signal on an integrated circuit on which the PLL is fabricated;
- (b) selecting a loop filter capacitance for the PLL from a plurality of selectable loop filter capacitances as a function of the range select signal; ~~and~~
- (c) enabling a first of a plurality of voltage-controlled oscillators (VCOs) in the PLL and disabling all other VCOs in the plurality as a function of the range select signal; and
- (d) converting differential signals produced at an output of each respective VCO, when enabled, into a digital logic level signal by a respective voltage level shifter, wherein each voltage level shifter comprises a power down input and at least one current source or voltage bias generator, which is enabled and disabled by the power down input .

20. (Currently Amended) The method of claim 19 wherein ~~(e)~~ the step of disabling all other VCOs comprises powering down at least one current source or voltage bias generator the other VCOs in the plurality as a function of the range select signal.